which may be affected by external magnetic fields include a magnetic random access memory device;

a first magnetic field shielding material in contact with said back surface of said chip; and

a second magnetic field shielding material in contact with said chip carrier, such that said magnetic random access memory device is located between said first and second magnetic field shielding materials.

2. (Amended) The structure of claim 1, wherein said first shielding material is in the form of a first layer of said magnetic field shielding material on said back surface.

3. (Amended) The structure of claim 1, wherein said first shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

Cancel claims 9, 10 and 12, without prejudice.

Rewrite claim 13 as follows:

13. (Amended) The structure of claim 11, wherein said second magnetic field shielding layer comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

Cancel claims 32-40, without prejudice.

Rewrite claims 64 and 70-76 as follows:

64. (Amended) An integrated circuit structure comprising:

a die carrier;

a die electrically connected to said die carrier, said die being in contact with a

Cancel B3

first layer of magnetic field shielding material, said die further comprising a magnetic random access memory device; and

a printed circuit board electrically connected to said die carrier, said printed circuit board being in contact with a second layer of magnetic field shielding material, and wherein said magnetic random access memory device is located between said first and second layers of magnetic field shielding material.

B4 35 ~~70~~. (Twice Amended) A method of packaging a semiconductor device comprising:

electrically coupling a die carrier to a first surface of a die, said first surface being opposite to a second surface of said die, and wherein said die includes a magnetic random access memory device;

contacting said second surface of said die with a first layer of magnetic field shielding material which shields said die from external magnetic fields, wherein said second surface is a back surface of the die; and

contacting said die carrier with a second layer of magnetic field shielding material which shields said die from external magnetic fields, such that said memory device is located between said first and second layers of magnetic field shielding material.

B5 36 ~~71~~. (Amended) The method of claim 35 ~~70~~ further comprising the act of electrically coupling said die carrier to a printed circuit board.

37 ~~72~~. (Amended) The method of claim 36 ~~71~~, wherein a third layer of magnetic field shielding material is formed on a surface of said printed circuit board.

38 ~~73~~. (Amended) The method of claim 37 ~~72~~, wherein said third layer of magnetic field shielding material is formed on a top surface of said printed circuit board.

39 ~~74~~. (Amended) The method of claim 37 ~~72~~, wherein said third layer of magnetic field shielding material is formed on a bottom surface of said printed circuit board.

40 77. (Amended) The method of claim 37, wherein said third layer of magnetic field shielding material is embedded within said printed circuit board.

cancel 85

41 78. (Amended) The method of claim 37, wherein said third layer of magnetic field shielding material is formed on both a bottom surface and a top surface of said printed circuit board.

Cancel claims 77 and 78, without prejudice.